

Appl. No. 10/697,137  
Reply to Office action of 11/28/2005

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A method for fabricating an integrated circuit, comprising the steps of:

- forming a dielectric layer;
- forming openings in the dielectric layer;
- filling said openings with a barrier, a copper seed, and an electroplated copper film;
- chemically-mechanically polishing said copper film; and
- after chemically-mechanically polishing said copper film, gaseously doping the copper film with silicon without forming a copper silicide by flowing a gas chemistry consisting essentially of silane over the copper film.

2. (original) The method of claim 1, wherein said doping step dopes only a top region of the copper film with silicon.

3. (currently amended) A method for fabricating an integrated circuit, comprising the steps of:

- forming a dielectric layer;
- forming openings in the dielectric layer;
- filling said openings with a barrier, a copper seed, and an electroplated copper film;
- chemically-mechanically polishing said copper film; and
- after chemically-mechanically polishing said copper film, gaseously doping the copper film with silicon without forming a copper silicide by flowing a gas chemistry consisting essentially of silane over the copper film with an RF power off.

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wherein said doping step dopes a surface of said copper film that leads to a final bulk silicon concentration in the range of 0.03at. % to 0.5 at. %.

4. (original) The method of claim 1, wherein said dielectric layer comprises an interlevel dielectric and an intrametal dielectric.

5. (original) The method of claim 4, wherein said openings comprise vias in the interlevel dielectric and trenches in the intrametal dielectric.

6. (original) The method of claim 1, wherein said doping step comprises flowing silane over the copper film for a duration in the range of 0.5 to 5 seconds at 325°C -425°C.

7. (currently amended) A method of fabricating an integrated circuit, comprising the steps of:

providing a semiconductor body having a trench formed in a dielectric layer at a surface thereof;

forming a copper film over the semiconductor body including with said trench,

chemically-mechanically polishing the copper film to form a copper interconnect;

after said chemical-mechanical polish step, doping said copper interconnect with silicon without forming a silicide by flowing silane over a surface of the copper interconnect with an RF power off prior to striking a plasma.

8. (cancelled).

9. (previously presented) The method of claim 7, wherein said silane is flowed over the surface of the copper interconnect for a duration of approximately 3 seconds.

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10. (previously presented) The method of claim 7, wherein said silane is flowed over the surface of the copper interconnect for a duration in the range of 0.05 to 5 seconds at 325°C to 425°C.

11. (original) The method of claim 7, wherein said doping step comprises part of a silicon nitride deposition process.

12. (previously presented) The method of claim 11, wherein said silicon nitride deposition process comprises the steps of:

- transferring the semiconductor body to a chamber;
- performing said doping step by flowing silane in said chamber for a given time prior striking said plasma in said chamber;
- striking said plasma in said chamber after flowing said silane for at least 0.5 seconds; and
- then flowing at least one nitrogen-containing source gas into said chamber to deposit a silicon nitride layer over said copper interconnect.